AMENDMENTS TO THE CLAIMS

1. (Original) A network storage apparatus for connecting a host computer with at least one storage device, comprising:

a passive backplane having a plurality of data buses including first and second data buses;

at least first and second channel interface modules, connected to said passive backplane and adapted to be connected to the host computer and the at least one storage device, that are operational to send and receive storage data to and from the host computer and the at least one storage device and that are operational to selectively transfer the storage data to one or more of said plurality of data buses; and

at least first and second controller memory modules, connected to said passive backplane, that communicate with said channel interface modules via said passive backplane, and that store and process the storage data transferred to and from said channel interface modules; wherein

at least said first channel interface module has a first switched path and a second switched path in which said first switched path is enabled to connect said first switched path to said first controller memory module and in which said second switched path to said second controller memory module using said passive backplane is disabled.

2. (Original) The apparatus of Claim 1, wherein:

at least said first channel interface module includes a communication path portion and a channel interface portion, wherein said channel interface portion is operable to transfer the storage data between the host computer and/or the at least one storage device and said communication path portion, and said communication path portion is operational to selectively transfer the storage data between said channel interface portion and said passive backplane.

3. (Original) The apparatus of Claim 1, wherein:

at least said first controller memory module includes a bus interface portion that connects to said passive backplane, a memory for temporary storage of said storage data, and a processing portion that organizes and arranges said storage data.

4. (Original) The apparatus of Claim 3, wherein said bus interface portion includes:

at least one backplane interface that connects to said passive backplane;

a memory interface that connects to said memory;

a processing interface that connects to said processing portion;

a bridge core that contains control logic operable to connect said processing interface, memory interface and backplane interface; and

at least one of an exclusive OR (XOR) engine that performs XOR functions on data blocks, and a direct memory access (DMA) engine that provides DMA access to said passive backplane.

5. (Currently Amended) The network storage apparatus of Claim 1, wherein said passive backplane further includes:

third and fourth data buses, wherein said first channel interface module is connected to a first two of said data buses, and wherein said second channel interface module is connected to a second of two of said data buses.

6. (Original) The apparatus of Claim 1, wherein each of said first and second data buses is part of a group of backplane buses and said group includes peripheral component interconnect (PCIX) buses.

7. (Original) The apparatus of Claim 2, wherein:

said passive backplane further includes a third data bus and a fourth data bus;

said first channel interface module includes a first bus port and a second bus port, and said second channel interface module includes a third bus port and a fourth bus port, said first, second, third and fourth bus ports being operable to connect said communication path portion to said passive backplane; and

said first controller memory module includes a first bus interface and a second bus interface, and said second controller memory module includes a third bus interface and a fourth bus interface, said first, second, third and fourth bus interfaces being operable to connect said controller memory module to said first, second, third and fourth data buses of said passive backplane.

8. (Original) The apparatus of Claim 7, wherein

said first bus port is connected to said first data bus and said second bus port is connected to said third data bus;

said third bus port is connected to said second data bus and said fourth bus port is connected to said fourth data bus;

said first bus interface is connected to said first data bus and said second bus interface is connected to said second data bus; and

said third bus interface is connected to said third data bus and said fourth bus interface is connected to said fourth data bus.

9. (Original) The apparatus of Claim 8, wherein:

said communication path portion of said first channel interface module has a first shared path, a first switched path and a second switched path; and

said communication path portion of said second channel interface module has a second shared path, a third switched path and a fourth switched path and in which:

said first shared path is connected to said first bus port and said second bus port;

said first switched path is connected to said first bus port and said channel interface portion;

said second switched path is connected to said second bus port and said channel interface portion;

said second shared path is connected to said third bus port and said fourth bus port;

said third switched path is connected to said third bus port and said channel interface portion; and

said fourth switched path is connected to said fourth bus port and said channel interface portion; and wherein

said first, second, third and fourth switched paths are operable to enable and disable communications involving said channel interface portion.

10. (Original) The apparatus of Claim 1, wherein:

said second switched path is enabled and said first switched path is disabled after a failure of said first controller memory module is detected using said second controller memory module.

11. (Currently Amended) A method for zoning a controller memory module to a channel interface module, comprising:

providing a first channel interface module having a first switched path and a second switched path;

connecting said first switched path to a first controller memory module using a passive backplane and said second switched path to a second controller memory module using said passive backplane;

enabling said first switched path; ~~and~~

disabling said second switched path;

sending data to said first controller memory module over said first switched path and said passive backplane, wherein said data is modified by said first controller memory module; and

receiving modified data from said first controller memory module over said first switched path and said passive backplane.

12. (Currently Amended) ~~The~~ A method ~~of Claim 11, further~~ for zoning a controller memory module to a channel interface module, comprising:

providing a first channel interface module having a first switched path and a second switched path;

connecting said first switched path to a first controller memory module using a passive backplane and said second switched path to a second controller memory module using said passive backplane;

enabling said first switched path;

disabling said second switched path;

providing a second channel interface module having a third switched path and a fourth switched path;

connecting said third switched path to said first controller memory module using said passive backplane and said fourth switched path to said second controller memory module using said passive backplane;

enabling said fourth switched path; and

disabling said third switched path.

13. (Original) The method of Claim 12, further comprising:

detecting a failure of said second controller memory module using said first controller memory module;

discontinuing any use of said second controller memory module;

enabling said second switched path; and

disabling said first switched path.

14. (Currently Amended) The method of Claim ~~11~~ 12, wherein said detecting [[step]] comprises:

monitoring a heartbeat of said second controller memory module using said first controller memory module; and

observing an irregularity in said heartbeat of said second controller memory module using said first controller memory module.

15. (Currently Amended) ~~The method of Claim 11,~~ A method for zoning a controller memory module to a channel interface module, comprising:

providing a first channel interface module having a first switched path and a second switched path;

connecting said first switched path to a first controller memory module using a passive backplane and said second switched path to a second controller memory module using said passive backplane;

enabling said first switched path;

disabling said second switched path;

discontinuing any use of said second controller memory module, wherein said discontinuing ~~step comprises~~ includes:

transmitting a failure signal from said first controller memory module to said second controller memory module;

receiving said failure signal at said second controller memory module; and

stopping operation of said second controller memory module.

16. (Currently Amended) ~~The method of Claim 11, further~~ A method for zoning a controller memory module to a channel interface module, comprising:

providing a first channel interface module having a first switched path and a second switched path;

connecting said first switched path to a first controller memory module using a passive backplane and said second switched path to a second controller memory module using said passive backplane;

enabling said first switched path;

disabling said second switched path;

detecting a failure of said first controller memory module using said second controller memory module;

incapacitating said first controller memory module;

enabling said second switched path; and

disabling said first switched path.

17. (Currently Amended) ~~The method of Claim 11, further~~ A method for zoning a controller memory module to a channel interface module, comprising:

providing a first channel interface module having a first switched path and a second switched path;

connecting said first switched path to a first controller memory module using a passive backplane and said second switched path to a second controller memory module using said passive backplane;

enabling said first switched path;

disabling said second switched path;

providing a second channel interface module having a third switched path and a fourth switched path;

connecting said third switched path to said first controller memory module using said passive backplane and said fourth switched path to said second controller memory module using said passive backplane;

detecting a failure of said first channel interface module using said first controller memory module;

incapacitating said first channel interface module; and

enabling said third switched path.

18. (Original) The method of Claim 17, further comprising:

idling said first controller memory module.

19. (Original) The method of Claim 17, wherein said detecting step includes:

performing run time diagnostics at said first channel interface module;

monitoring results of said run time diagnostics at said first controller memory module; and

observing an irregularity in said results.

20. (Original) The method of Claim 17, wherein said incapacitating step includes:

transmitting a failure signal from said first controller memory module to said first channel interface module;

receiving said failure signal at said first channel interface module; and

discontinuing operations at said first channel interface module.

21. (Currently Amended) An apparatus in which a channel interface module is associated with a particular controller memory module, comprising:

at least a first channel interface module having a first switched path and a second switched path;

a passive backplane;

a first controller memory module connected to said first switched path using a first bus included in said passive backplane, said first controller memory module operable to form modified data received from said at least a first channel interface module over said first switched path and to return modified data to said at least a first channel interface module over said first switched path; and

a second controller memory module ~~disabled from~~ selectively connected to said second switched path using a second bus included in said passive backplane, said second controller memory module operable to form modified data received from said at least a first channel interface module over said second switched path and to return modified data to said at least a first channel interface module over said second switched path, wherein a first one of said first switched path and said second switched path is disabled when a second one of said first switched path and said second switched path is enabled.

22. (Original) The apparatus of Claim 21, wherein:

said second controller memory module detects a failure of said first controller memory module and is involved with disabling said first switched path and enabling said second switched path.

23. (Currently Amended) ~~The apparatus of Claim 21, further~~ An apparatus in which a channel interface module is associated with a particular controller memory module, comprising:

at least a first channel interface module having a first switched path and a second switched path;

a passive backplane;

a first controller memory module connected to said first switched path using said passive backplane;

a second controller memory module disabled from said second switched path; and

a second channel interface module having a third switched path and a fourth switched path and in which said second controller memory module is connected to said fourth switched path using said passive backplane while said third switched path is disabled.

24. (Original) The apparatus of Claim 23, wherein:

said third switched path is enabled when a failure of said first channel interface module is detected using said first controller memory module.